

LeCroy

CAMAC Model 8800
Memory Module

instrumentation
for the study of
transient phenomena

PALO ALTO, CA.



technical information manual

CAMAC Model 8800 Memory Module

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy / CALIFORNIA
PALO ALTO, CALIFORNIA

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Palo Alto, CA, telephone 415-328-3750, or from your local distributor in countries other than the U.S.A.

LeCROY RESEARCH SYSTEMS

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TECHNICAL DATA

LeCroy



CAMAC Model 8800 Series Memory Modules

The 8800 Series memory modules have been developed for compatible use with LeCroy fast Transient Recorders, Video Digitizers, and Data Loggers. The basic module is designed for 12-bit X 32K storage, allowing common circuitry to accommodate the appropriate number of 1 X 16K dynamic RAM's. This technique offers the convenience of common operating characteristics and common components for a variety of fast to slow data acquisition devices now available for transient signal recording and analysis.

The modules comprising the 8800 Series are identified below with their relevant assignments:

Model 8800/8	8-bit X 32K--Designed for usage with Model 2264 Multi-channel Waveform Digitizer.--One or more modules required depending on memory capacity desired.
Model 8800/8V 8800/9V	8-bit or 9-bit X 32K--Designed for usage with Model 8258 20 MHz Video Digitizer.--Four modules are required for operation up to 20 MHz; 2 for operation up to 10 MHz.
Model 8800/10	10-bit X 32K--Designed for usage with Model 8210 10-bit, 1 MHz Waveform Digitizer.--One or more modules required depending on memory capacity desired.
Model 8800/12	12-bit X 32K--Designed for usage with LeCroy Model 8212, 32-Channel 12-Bit Fast Data Logger.--One or more modules required depending on memory capacity desired.

January 1980

*Instrumentation for the study
of transient phenomena*

SPECIFICATIONS

CAMAC

MEMORY MODULES

Model 8800

Inputs:

TTL Levels. Lines: 12 data, 12 grounds; 7 control lines, 7 grounds. One 40-conductor edge connector located at the upper rear of the module. Mates with LeCroy Model DC8800/nm Data Cable (where "n" equals the number of memory modules linked to one data acquisition device and "m" equals feet of cable between the device and the first 8800 module).

Memory Organization:

Read/Write operations are controlled by the companion digitizer. Data from the A/D converter is sequentially written into the memory module. Readout into the CAMAC dataway is also sequential with the last word written being the last word read. Readout starts at the first word of each memory block (the amount of memory per active A/D channel).

Readout is non-destructive and the memory is protected against write operations from the CAMAC dataway. It can be written only from the A/D converter.

Memory Active Light:

Front-Panel LED indicates when memory is being loaded or read.

Memory Size:

32,768 words. 8, 9, 10 or 12 bits.

Memory Expansion:

Serial organization permits adding Model 8800 modules in a daisy-chained fashion with the maximum memory size dictated by the control board of the ADC module. Memory size must be internally specified on the control board of the "front end" ADC (jumper option) and on the memory modules (onboard Programming Switch). The LeCroy Model 2264 and 8210 can drive 3 modules (Model 8212, 4 modules) with larger memory extension possible as a factory option.

The Model 8258 digitizer utilizes memory modules in blocks of either 2 (for operation at rates up to 10 MHz) or 4 (for operation at rates up to 20 MHz). Up to 16 such blocks (32 or 64 modules) can be driven by a Model 8258.

Packaging:

In conformance with the international CAMAC standard for nuclear modules (European ESONE Report #EUR4100 or U.S. IEEE Report #583). RF-shielded CAMAC #1 module.

Power Supplies:

The Model 8800 Series can draw +12 volts from the +12 volt CAMAC bus or can be jumpered internally to use a built-in +24 to +12 volt converter. Since the memory is not read directly, it can be located in an adjacent power crate (<4 feet of cable) with only +12, +6 volt power.

Power Consumption:

Voltage	Bits	MA	Watts
+12 (or +24)	8	320	3.8 (7.7)
	9	360	4.3 (8.6)
	10	400	4.8 (9.6)
	12	490	5.9 (11.8)
+6	all bits	650	3.9
-6	all bits	30	0.2

Bits	Total Watts with +12 V	Total Watts with +24 V
8	7.9	11.8
9	8.4	12.7
10	8.9	13.7
12	10.0	15.9

CAMAC Model 8800/X*

32K Memory Module

LeCroy
8800
MEMORY
MODULE



← LED lights when memory is enabled.

Memory is CMOS 16K dynamic RAM with a rate capability of 4-5 MHz.

Note: LeCroy Model 8800 is a general purpose memory module which can be used with several LeCroy transient digitizer. Customers who wish to increase the 8800 word size (ex. 8800/8 to 8800/12) may return the unit(s) to the factory for updating. Charges will be made only for additional memory and new P.C. board.

* X designates the number of bits on an actual module.

4. OPERATIONAL DESCRIPTION

4a. General

The LeCroy 8800/X series memory modules are 8-bit (Model 8800/8), 10 bit (Model 8800/10) and 12 bit (8800/12) word dynamic memories with a capacity of 32,768 words. They are designed especially for high speed sequential storage of data. The input data is multiplexed into two banks of 16K dynamic RAM memory and is written into the memories in a page mode memory cycle as the memories are addressed by on board counters. During readout the data is multiplexed onto the I/O lines from the two memory banks in the same order that it was written into the memory. The entire memory (per digitizer channel) must be read out to reach the last word written.

Since these units are dynamic RAM's, the 128 rows in the memory banks must all be addressed at least once every 2 msec. When memory cycles occur at a rate too low to satisfy this condition, refresh cycles must be inserted into the series of operations by appropriately timed refresh pulses on the Model 8800/X refresh control line. Multiplexing of the data into the memory and memory cycles are controlled by pulses on the memory strobe line. Read or write operation is determined by the logic level on the read/write control line. The logic circuits are reset or initialized by a TTL low pulse on the initialize line. In addition, these units are designed so that they may be cascaded to increase memory size. To facilitate this mode of operation, each module has two memory enable lines and a memory enable return line. All of the above mentioned control lines as well as the I/O lines for the data are connected to through a rear panel 40 pin header.

4b. Front Panel Indicator

LED lamp lights when memory module is enabled for read or write operations. When cascaded memory modules are being used, this allows the user to see which module is currently receiving or dispensing data.

4c. Programming Switches

Seven switches in a DIP package are accessible through a window in the side cover of the 8800/X. Five of the switches are used to program the module for a position in a chain of modules, i.e., the switch positions will determine whether the module is to function in a first, last or intermediate position in the chain. The remaining two switches program the scanning of the memory addresses to be either by row or by column. See page 5.1 for complete instructions for switch settings.

4d. Rear Edge Connector Signals

- MEM EN 1: TTL low, indicates the module has been completely written or read. This signal is used to enable the next 8800 to read or write data. Maximum signal duration is approximately 150 nsec, minimum approximately 100 nsec.
- MEM EN RTN: Same as MEM EN 1 except this signal is transmitted back to the digitizer module's controller. MEM EN RTN is generated by the last memory module on the bus (see section 5a).
- REFRESH: TTL high pulse, minimum duration is 200 nsec. This signal initiates a refresh cycle in the memory module.
- CLOCK: TTL high pulse, minimum duration is 50 nsec. This signal stores data in the input latches during write operations. Alternate clock pulses initiate memory cycles. During readout the signal alternately enables bank #1 and #2 output latches (see functional description) and alternate clock pulses will initiate memory cycles.
- R/W: TTL high to write, low to read. Transition from high to low initiates memory cycle which locks data into output latches.
- INITIATE: Minimum 400 nsec pulse to initialize memory address registers to zero and reset internal logic.
- DATA LINES ($2^{11} \rightarrow 2^0$): Bidirectional TTL data, 2^{11} is the MSB and 2^0 is the LSB.
- MEM EN 2: Same as MEN EN 1.

4e. Power

Since the 16K dynamic RAMs use +12 volts, an internal voltage regulator is supplied which will drop +24 volts to +12 volts. However, for CAMAC crates which supply power to their +12 V bus lines, the 8800 has internal jumpers (see schematic) allowing operation from +12 V which is in fact recommended due to lower total power dissipation.

The 8800 memory module uses no CAMAC control or data lines and may be placed in a dummy crate which contains power only. Consult factory concerning maximum bus cable lengths.

5. OPERATING INFORMATION

5a. Switch Settings (Refer to Block Diagram)

General Rules - A memory module may receive or generate memory enable pulses on either MEN1 or MEN2, but may not receive and generate on the same line; thus switches S1 and S6 or S2 and S7 should never be on simultaneously. The memory may either be scanned by row or column,* thus switches 3 and 4 should always be in opposite states. A memory system may consist of a series of memory modules. The last module in the series must send a memory enable return (MEN RTN) pulse to the controller signaling the end of a memory scan or the beginning of a new memory scan, therefore switch 5 must be on only in the last module in the series.

Specific Example - The following example system will illustrate the use of the memory enable lines and detailed switch settings. If a chain of four memory modules are to be used to scan by row (i.e., each column element in a row is addressed before advancing to the next row), set switch 4 on and switch 3 off on all of the units.

Module #1 must receive an enable pulse from the controller on MEN1, therefore, S2 must be on and S7 off. Module #1 must then send an enable pulse to Module #2 on MEN2, thus, S6 must be on and S1 off. To isolate the pulse on the MEN2 line from the controller, the MEN2 line between Module #1 and the controller must be cut.

Module #2 is receiving an enable pulse on MEN2; therefore S1 must be on and S6 off. Module #2 must now send an enable pulse to Module #3 on MEN1, thus S7 must be on and S2 off. To isolate this pulse on MEN1 from Module #1's MEN1 input, the MEN1 line between Module #1 and Module #2 must be cut.

Module #3 is receiving on MEN1, therefore S2 must be on and S7 off. The enable pulse to Module #4 must be sent on MEN2, thus S6 must be on and S1 off. To isolate this pulse from Module #2, the MEN2 line between Module #3 and Module #2 must be cut.

Module #4 is receiving on MEN2, therefore S1 must be on and S6 off. Since Module #4 is the last in the chain it must send a memory enable return pulse back to the controller, thus S5 must be on (S5 on the first three modules must be off). S2 and S7 could both be turned off to disconnect MEN1 between Module #3 and Module #4, but it is recommended that MEN1 be cut between these modules.

The MEN1 and MEN2 lines are the outside (upper and lower) control lines facilitating the necessary alternating cuts in these lines between units on the system.

* Scanning by column also requires an internal jumper connection (AG, pin 10)

6. FUNCTIONAL DESCRIPTION

6a. General

The LeCroy Model 8800 is a dual multiplexed memory consisting of 16K words per memory bank (32K total). The word size is stated on the front panel (8800/10 implies 32K words, each 10 bits wide) and the maximum size is 12 bits. Write or read operations can be executed up to a 5 MHz average rate (see timing diagrams). The memory is only sequentially addressable when writing or reading. Since the 8800 uses 16K dynamic RAMs, a minimum of 128 refresh pulses must be supplied every 2 msec. Refresh is accomplished by applying a 200 nsec (minimum) pulse to the refresh control line. The digitizer module's controller circuitry generates this pulse at a time which ensures that memory read/write and refresh cycles do not overlap.

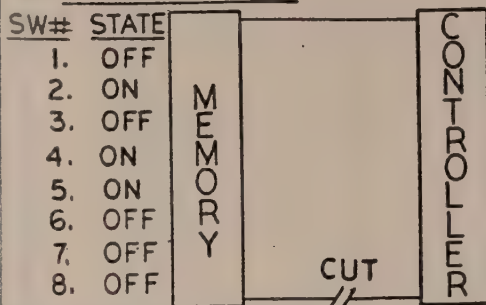
6b. Writing Data

After the memory has been initialized and enabled (see timing diagram) data can be written into memory. The first clock pulse will strobe data into the input storage register for Memory Bank #1 (see block diagram). The second clock pulse will strobe data into Memory Bank #2, transfer Memory Bank #1 storage register data to the input latch and initiate a 400 nsec memory cycle which stores data. This sequence continues until the memory is filled and MEM EN RTN or MEM EN $\frac{1}{2}$ is generated. After this time the internal logic will disable the memory write pulse.

6c. Reading Data

After the $\overline{R/W}$ control line changes state to a TTL low level, the 8800 will enter the readout mode. The $\overline{R/W}$ line transition initiates a memory readout cycle which loads data from the present memory address into Bank #1 and #2 output latches. At this time the input latches are disabled and Memory Bank #1's output latch is enabled onto the data bus. The first clock pulse will then disable Bank #1 output latch and enable Bank #2 output latch. The second clock pulse re-enables Bank #1 output latch, initiates a memory cycle and loads new data into the output latches. The sequence continues until the entire memory has been read out and MEM EN RTN or MEM EN $\frac{1}{2}$ is generated. After this time both output latches are disabled. (NOTE: During readout MEM EN RTN or MEM EN $\frac{1}{2}$ is generated immediately after the last two data words are stored in the output latches. The output latches will then automatically be disabled after the last two words have been readout).

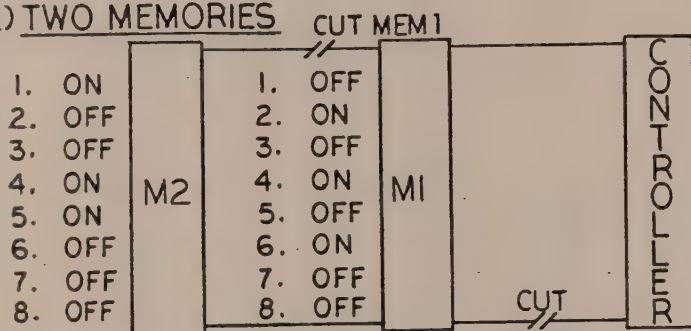
(1) ONE MEMORY



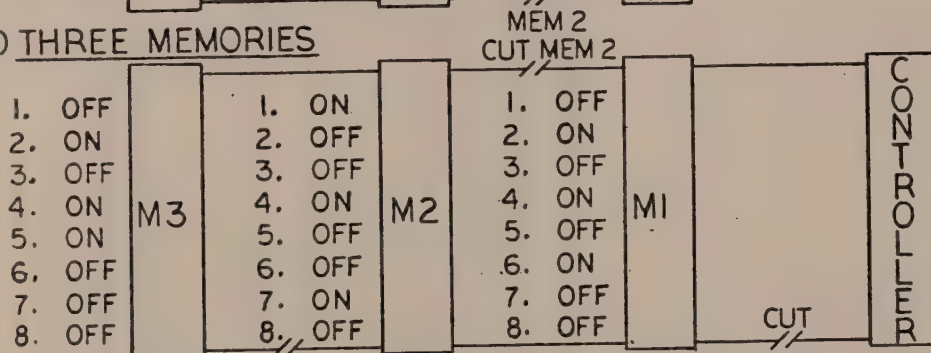
*FOR USE WITH MODEL 8258 VIDEO-DIGITIZER

NOTE APPLIES TO THESE SWITCHES ONLY
AND NOTE THAT NUMBER OF MEMORIES
MEANS IN EACH BRANCH.

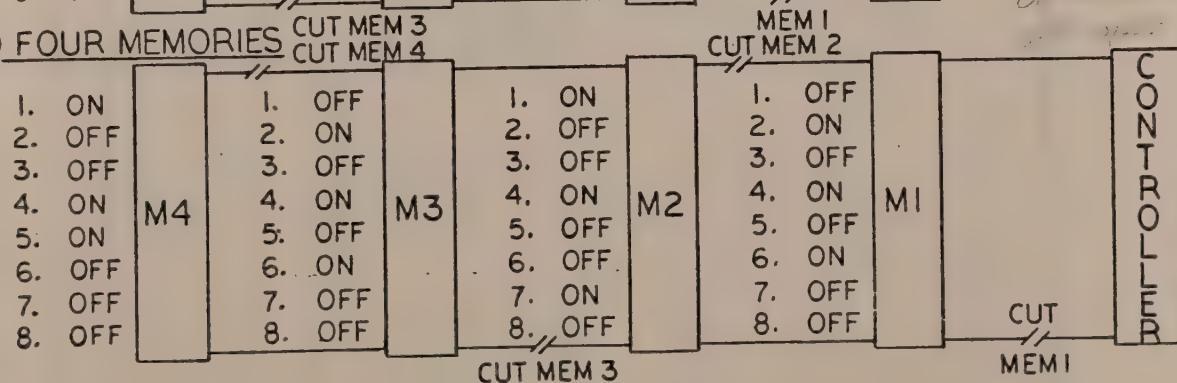
(2) TWO MEMORIES



(3) THREE MEMORIES

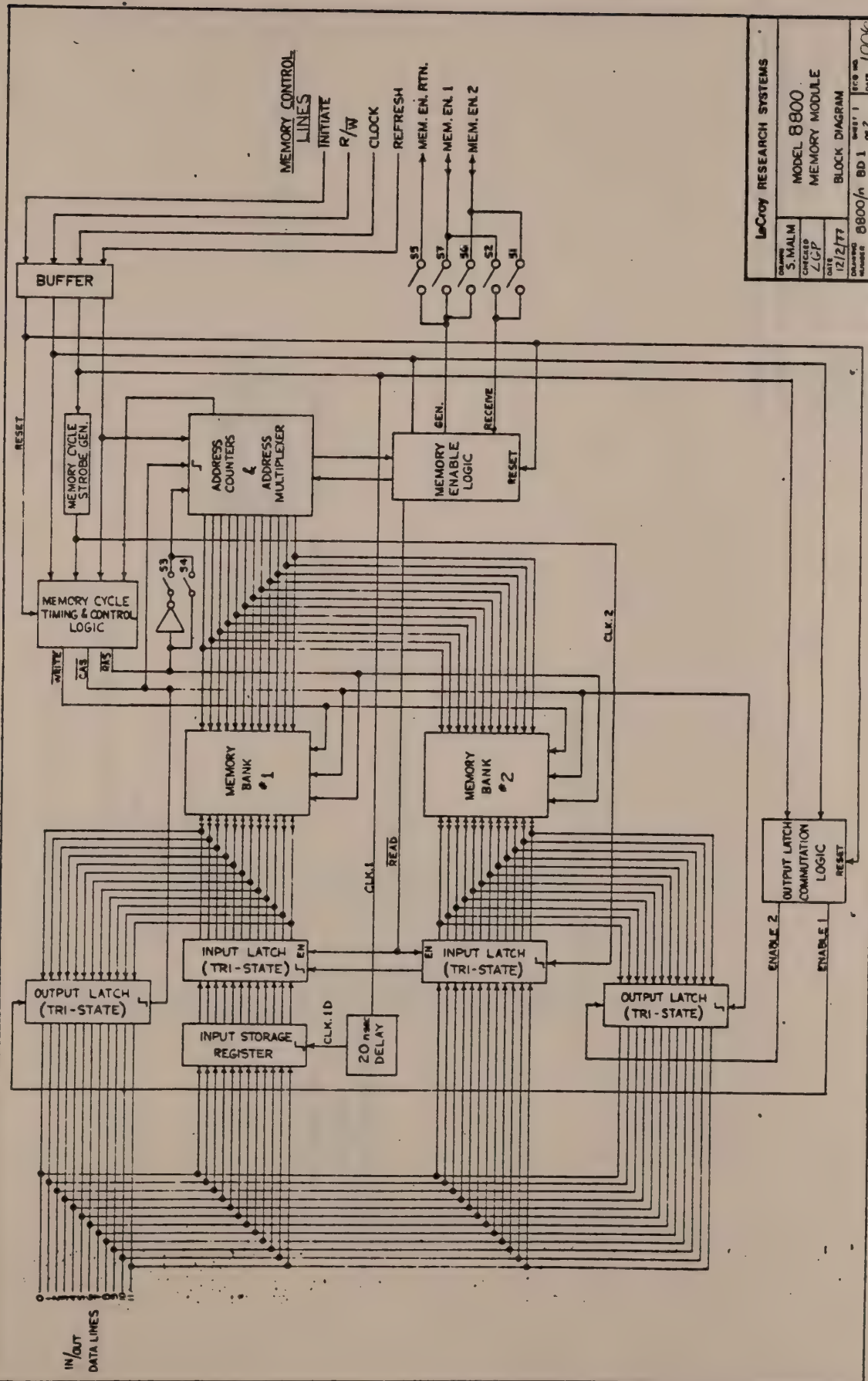


(4) FOUR MEMORIES

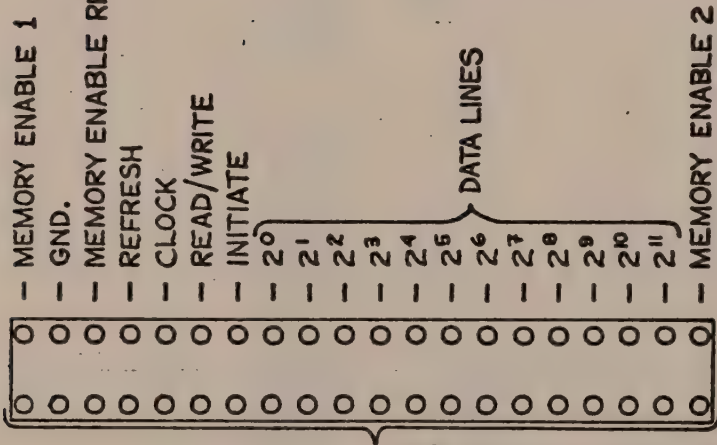


ECO NO. DATE

452	08-29-77	FINALIZED DOCUMENTATION.
467	09-19-77	GENERATED SEPARATE FRONT PANELS FOR 8, 9, 10, & 12, REDID LAYOUT TO IMPROVE NOISE IMMUNITY: BOARD REVISION LEVEL CHANGED FROM 2800/A TO 8800.
1001-1004	-	THESE #' NOT USED.
1005	07-27-78	8800 REAR PANEL MODIFICATION, ADDED PRE-ASSEMBLY #'S TO PARTS LIST.
1006	02-02-79	VALUES ASSIGNED TO RESISTORS 18 (5.1K), R20 (3.6K), SR22 (3.9K), CHANGES REFLECTED IN SCHEMATIC AND PARTS LIST.
1007	-	THIS # NOT USED.
1008	11-28-79	TVSI POLARITY REVERSED ON ASSY. DWG. C27 CORRECTION ON ASSY. DWG.
1009	12-04-79	8800-1 DELETED: #229-010-005 (2) ADDED: #229-020-055 (2) REFERENCE DESIGNATIONS REMAIN THE SAME.
1010	03-19-80	8800-1 UPDATE DWGS. TO PRODUCTION/TEST REQUIREMENTS.
REMARKS		LeCROY RESEARCH SYSTEMS CORPORATION DRAWN ENGINEERING CHECKED DATE CHANGE ORDERS MODEL 8800 DRAWING No.



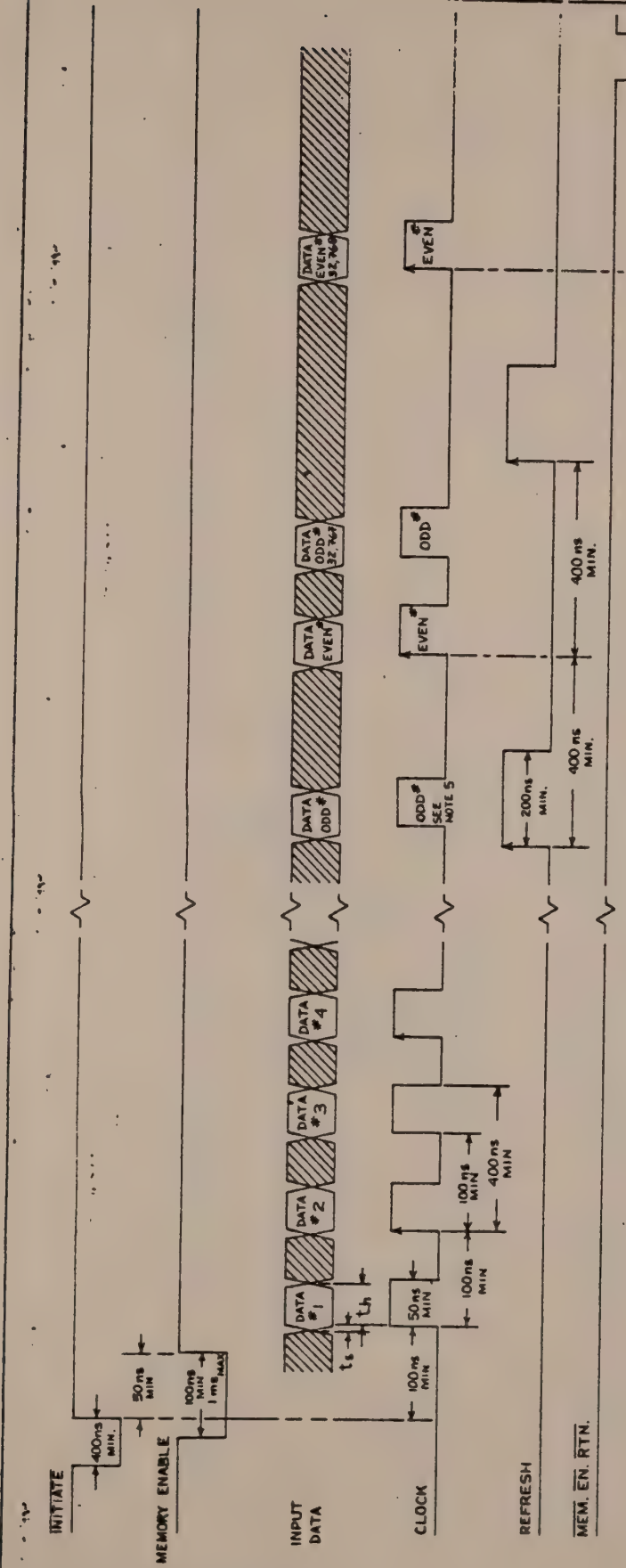
LeCroy RESEARCH SYSTEMS			
DESIGNED BY	S. MALM	MODEL	8800
CHECKED BY	ZCP	MEMORY MODULE	
DATE	12/2/77	BLOCK DIAGRAM	
DRAWING NUMBER	8800/m BD 1	SHEET 1 OF 2	100KHz



ALL PINS ON
THIS SIDE
ARE GROUNDED

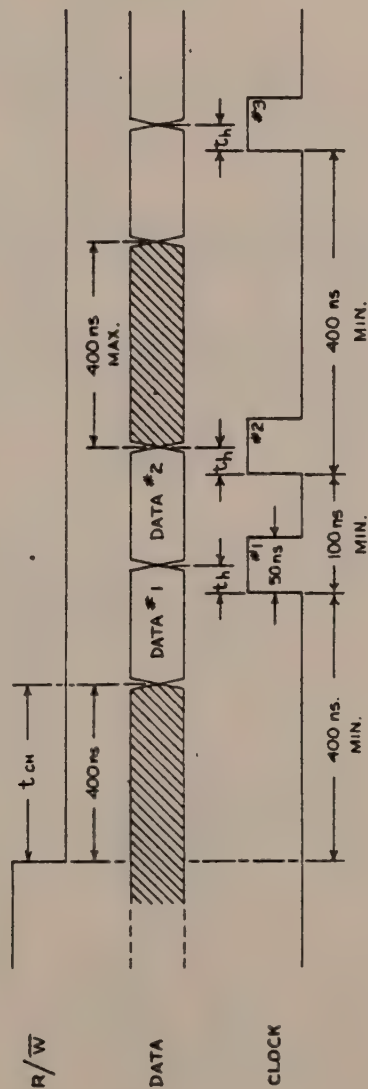
PIN ASSIGNMENTS
for REAR CONNECTOR
(REAR VIEW SHOWN)

LeCROY RESEARCH SYSTEMS CORPORATION WEST NYACK, NEW YORK	
DRAWN S.MALM	MODEL 8800 MEMORY MODULE
CHECKED LGP	BLOCK DIAGRAM
DATE 12/2/77	DRAWING No. 8800/n RD1 OF 2
SHT. 2 ECO No. 1006	



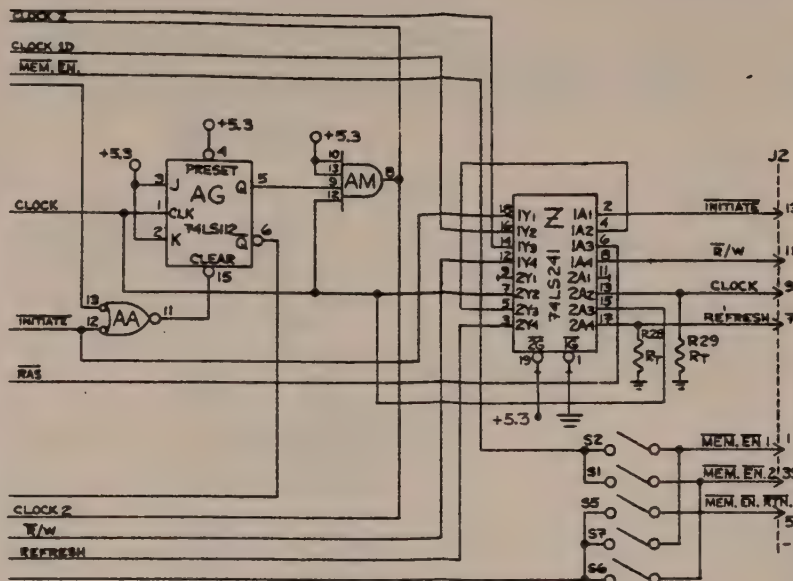
GENERAL TIMING RULES: (WITH R/W IN TTL HIGH STATE)

- 1) t_s : DATA MUST BE SET UP ON DATA LINES AT LEAST 20 ns BEFORE POSITIVE GOING CLOCK EDGES.
- 2) t_h : DATA MAY CHANGE 50 ns AFTER POSITIVE GOING CLOCK EDGES.
- 3) MEMORY CYCLES ARE INITIATED BY THE EVEN-NUMBERED CLOCK PULSES AND THE REFRESH PULSES (POSITIVE GOING EDGES, MARKED WITH ARROWS IN THE ABOVE DIAGRAM). THESE EDGES MUST BE SEPARATED BY A MINIMUM MEMORY CYCLE TIME OF 400 ns.
- 4) REFRESH PULSES: MINIMUM 200 ns DURATION (MINIMUM 128 PULSES EVERY 2 ms)
- 5) ONLY ODD-NUMBERED CLOCK PULSES MAY OCCUR DURING REFRESH.



GENERAL TIMING RULES: (WITH MEMORY WRITTEN INTO AS DESCRIBED IN 8800-TD1, SHEET 1)

- 1) t_{ch} : NO REFRESH OR CLOCK PULSES ARE ALLOWED DURING THIS TIME OR THE 400 ns PRECEDING THE R/W TRANSITION.
- 2) DATA #1 CORRESPONDS TO [LAST ODD DATA+1] WRITTEN INTO MEMORY.
- 3) t_h : ~ 20 ns
- 4) REFRESH TIMING AND CONDITIONS } SAME AS DURING WRITE OPERATIONS.
MEM. EN. RTN. " " " "



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LeCroy RESEARCH SYSTEMS

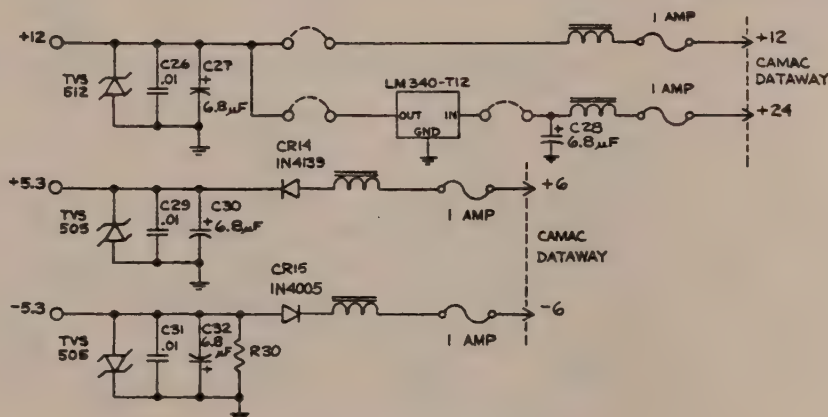
MODE - 8800

MEMORY MODULE

DESIGN S. MALM
CHECKED LCP
DATE 1/6/78
REVISION 5
OF 5
1010

SWITCH SETTINGS

MEM. EN.1	REC.	S2 ON S7 OFF
	GEN.	S2 OFF S7 ON
MEM. EN.2	REC.	S1 ON S6 OFF
	GEN.	S1 OFF S6 ON
MEM. EN. RTN.		S5 ON
ROW SCAN		S3 OFF S4 ON
COLUMN SCAN		S3 ON S4 OFF



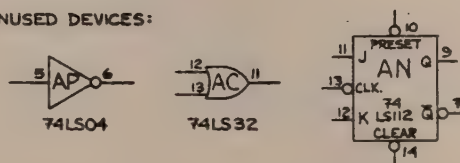
LeCroy * DESIGNATION -53 GND +53 +12

200-031-046	AB, AP	7	14
200-031-049	AH	7	14
200-031-057	AF	7	14
200-031-072	AM	7	14
200-031-073	AC	7	14
200-031-086	AA	7	14
200-041-017	AG, AN	7	14
200-041-026	T, U, X, W	8	16
200-041-039	AD	8	16
200-042-002	AJ	8	16
200-042-005	AE	8	16
200-071-002	Y, Z	10	20
200-071-003	A, C, D, G, H, K	10	20
206-062-116	A1-12, M1-12	1	16 9 B
206-091-242	AL	14	28
200-041-052	B, D, F	8	16

THIS SHEET ONLY:

HIGHEST REF. NUMBERS USED:
R30, C32, CR15
REF. NUMBERS OMITTED:
R31-, C33-, CR16-

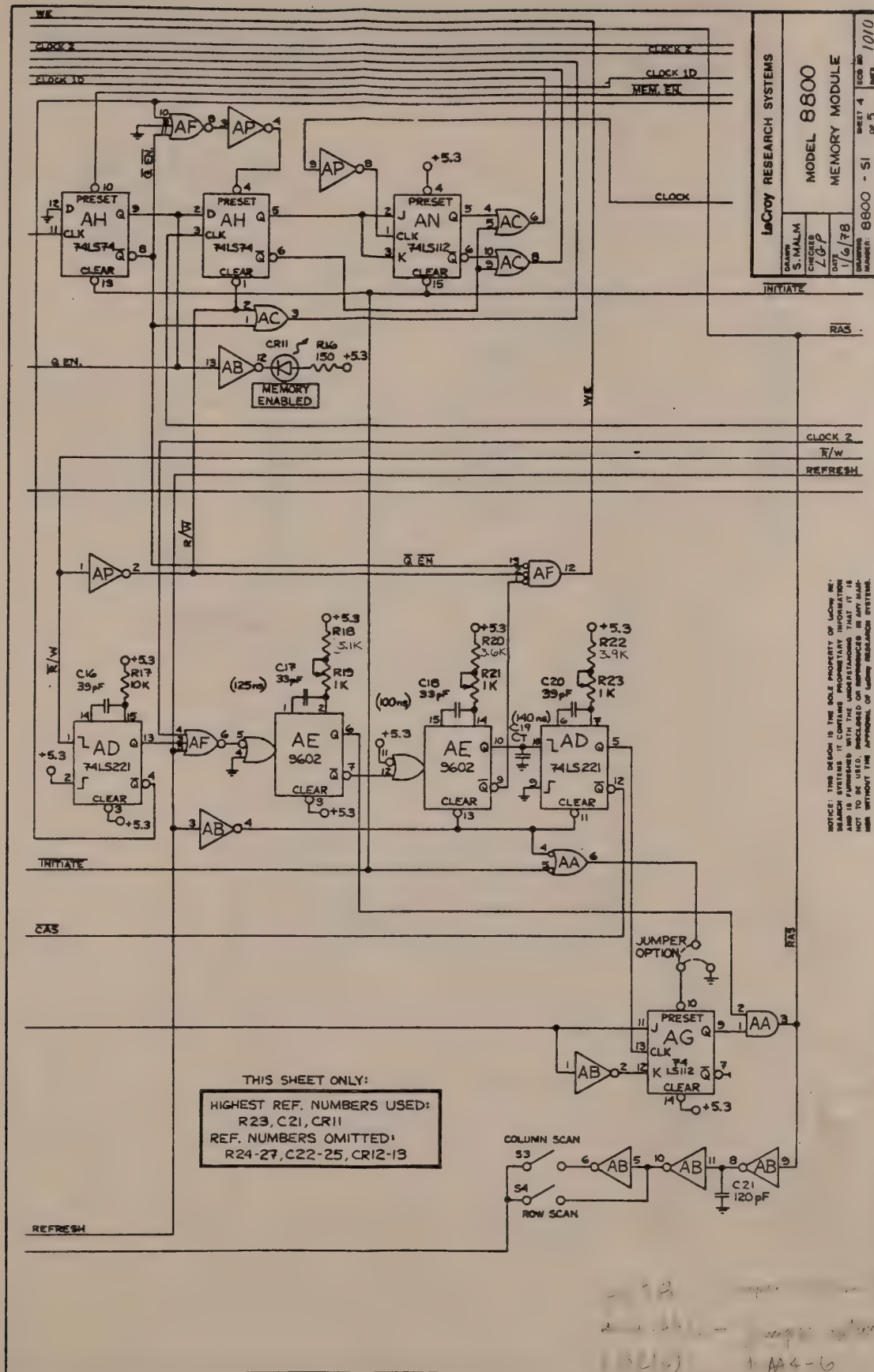
UNUSED DEVICES:



NOTES:

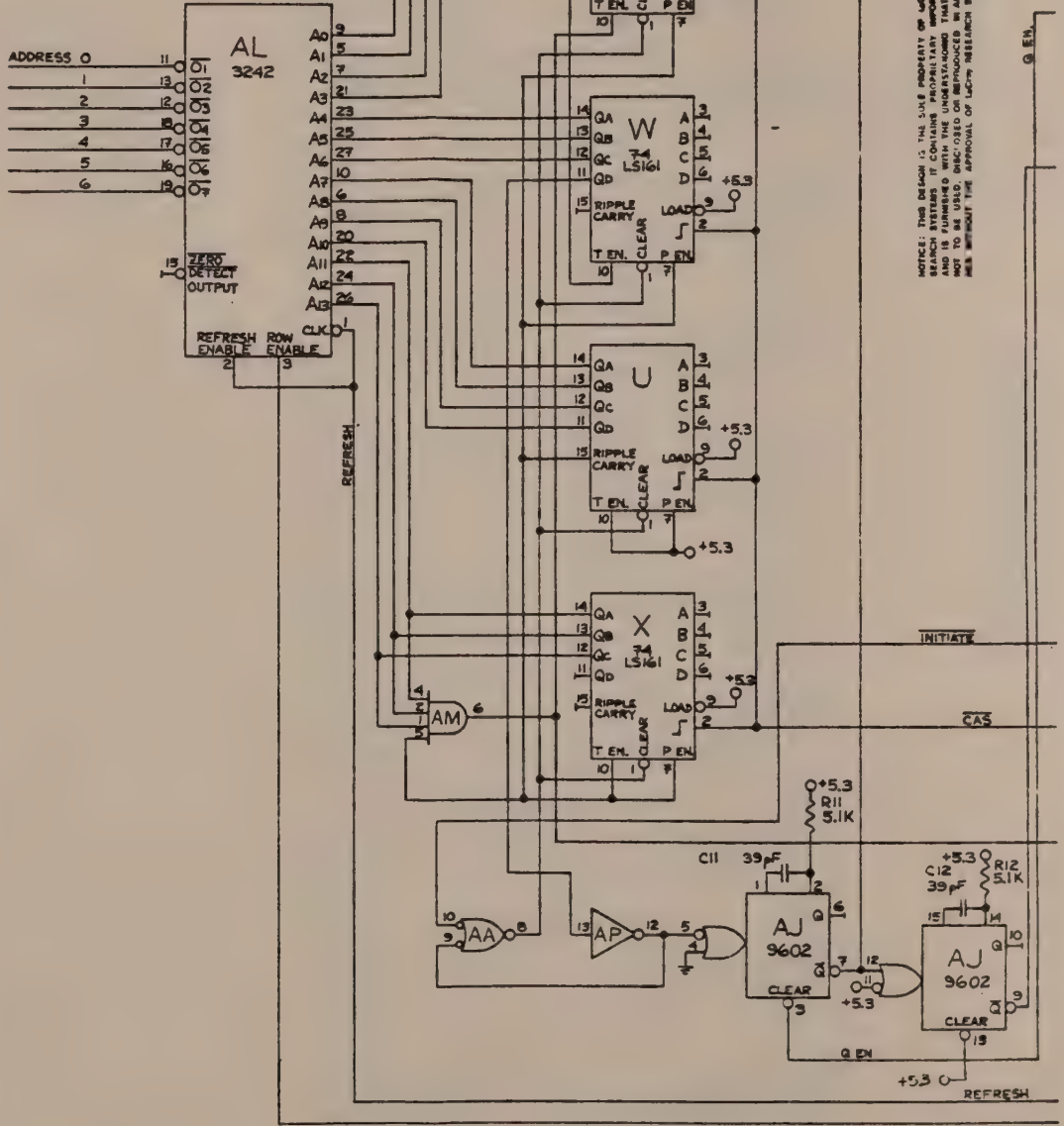
- NOTE 1 LOCATED ON SHEET 1
- ADDITIONAL .01μF AND/OR 6.8μF CAPACITORS MAY BE USED ON VOLTAGE BUSES, NOT SHOWN.
- * T DENOTES VALUE CHOSEN AT TEST.

UNIT	DEVICES NOT USED
8-BIT	B, D, F, A1, A2, A3, A4, M1, M2, M3, M4
9-BIT	A1, A2, A3, M1, M2, M3
10-BIT	A1, A2, M1, M2
12-BIT	



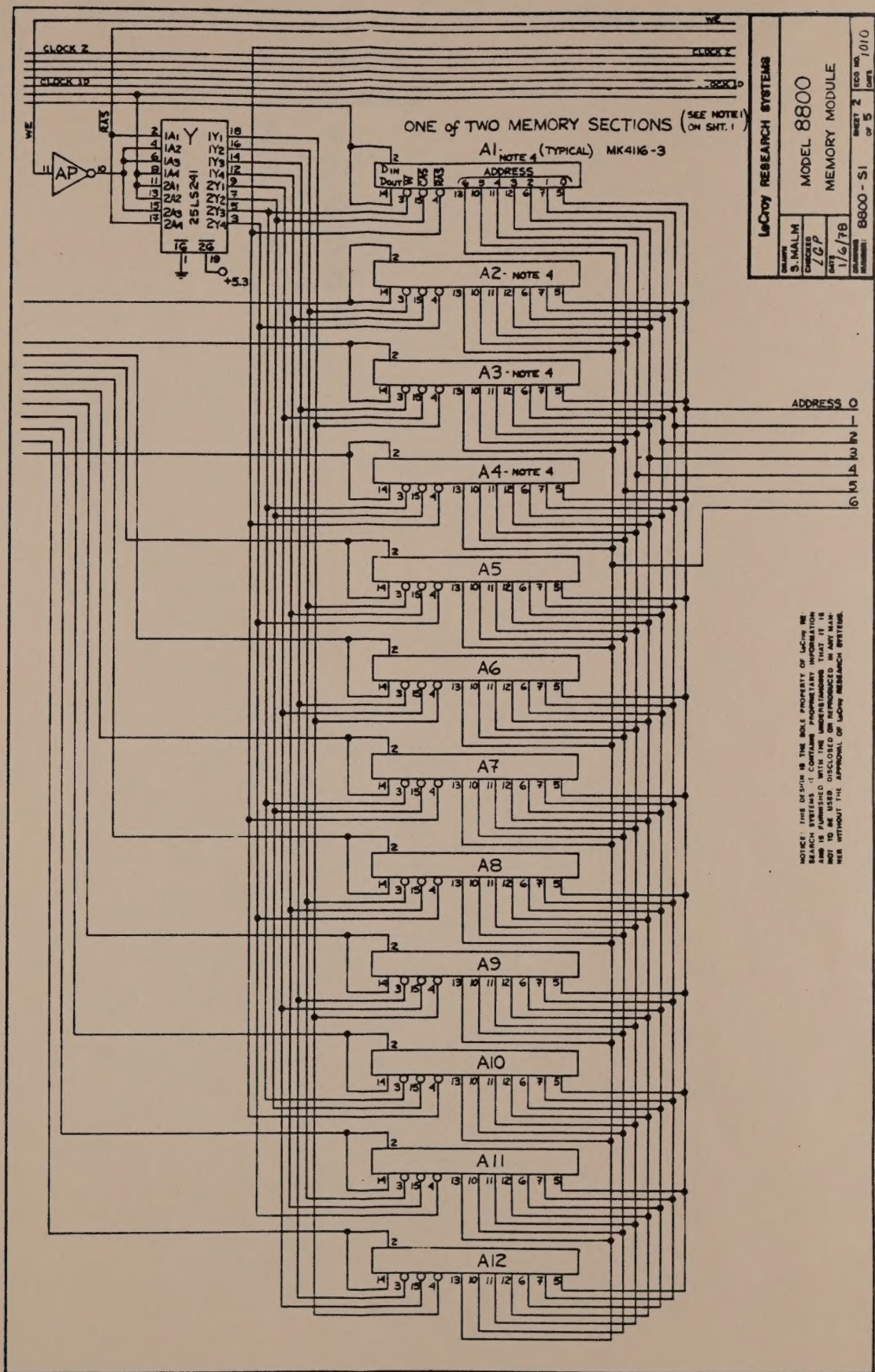
WE
CLOCK 2
CLOCK 10

THIS SHEET ONLY:
HIGHEST REF. NUMBERS USED:
R12, C12,
REF. NUMBERS OMITTED:
R13-15, C13-15,



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LECROY RESEARCH SYSTEMS			
DESIGN	S. M. L. M.	MODEL	8800
CHECKED	Z. G. P.	MEMORY MODULE	
DATE	1/6/78		
DRAWN			
CHECKED			
SHEET 3	OF 5	ECO NO.	1010
8800 - SI			



LeCroy RESEARCH SYSTEMS

DESIGNED BY S. MALIM	MODEL 8800
CHECKED BY ZGP	
DATE 1/6/78	MEMORY MODULE
REVISION (1)	

1000 1010
SHEET 2 OF 5

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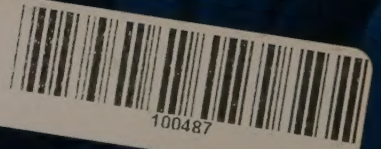
Switch settings for 8250 Digitizer (all 4 modules are the same)

1. Open
2. Closed
3. C
4. O
5. C
6. O
7. O
8. O

www.manualsplus.com



1033872



100487